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10/087,610	03/01/2002	Richard A. Nichols	100.152US01	7953

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EXAMINER	
WONG, LINDA	
ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,610	NICHOLS, RICHARD A.	
	Examiner	Art Unit	
	Linda Wong	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7-10,12,13,15-22,24-26,28 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7-10,12,13,15-22,24-26,28 and 30-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments, see Applicant's Remarks, filed 2/16/2006, with respect to the rejection(s) of claim(s) 1-2,4-5,7-10,12-13,15-17,19-22,24-26,28,30-34 under Irwin in view of Yamamoto et al have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Zhang et al (US Patent No.: 6304582) in view of Zampetti et al (US Patent No.: 6943609).

Claim Objections

2. **Claim 1** is objected to because of the following informalities: Claim 1 recites the limitation of "an expected quality level". After further review of the specification, it seems the applicant is comparing the quality level of the reference clock signal with the quality level of the phase locked loop, which is constantly changing. Since the quality level of the phase locked loop is constantly changing, it cannot be considered expected. Thus, it suggested by the examiner to eliminate the term "expected". Appropriate correction is required.
3. **Claims 28, and 34** are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 26 and 33, respectively. (Claim 28 is equivalent to claim 26 and Claim 34 is equivalent to claim 33) When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object

to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1,2,4,5,7,8,9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al (US Patent No.: 6304582) in view of Zampetti et al (US Patent No.: 6943609).

   a. **Claim 1**, Zhang et al discloses a phase comparator (Fig. 3, label 210) having a first input for receiving a reference clock signal (Fig. 3, labels 4kHz and T1 clocks), a second input for receiving a feedback signal (Fig. 3, label 275), and an output for providing an error signal (Fig. 3, labels 12 bits and 210), a loop filter (Fig. 3, label 265) having an input for receiving the error signal (Fig. 3, labels 210 and 12 bits) and an output for providing a control signal (Fig. 3, output from label 265), an oscillator having an input for receiving the control signal and an output for providing a timing signal (Fig. 3, label 270, output from label 270 and output from label 265), wherein the feedback signal is derived from the timing signal (Fig. 3, label 273 and 275 and 4kHz), a processor coupled to the oscillator (Fig. 3, label 240 and Col. 9, lines 13-21), wherein the processor is further coupled to receive a status message indicative of a quality

level of the reference clock signal (Fig. 3, label 235, Col. 10, lines 32-43, Col. 11, lines 56-63, Col. 12, lines 34-40 and Col. 14, lines 14-30) and a memory coupled to the processor (Col. 9, lines 14-21), wherein the memory has instructions stored, wherein the instructions stored on the memory are capable of causing the processor to place the phase locked loop in the holdover condition (Col. 19, lines 4-41, Col. 14, lines 10-40 and Col. 13, lines 48-51) when a quality level of the reference clock signal (Col. 19, lines 22-28) indicated by the status message (Col. 19, lines 9-13, Col. 14, lines 10-40 and Col. 13, lines 48-51) is less than a quality level (Fig. 8, label aging conditions and meet conditions to update DAC_in_aging?, Col. 19, lines 9-34 and Col. 14, lines 14-40) of the phase locked loop in the holdover condition. Although Zhang et al does not explicitly state a machine- readable medium, a machine-readable medium is a well known type of memory used in processors. It would be obvious to one skilled in the art to use a machine-readable medium as a memory based on the designer's choice. Although Zhang et al does not explicitly state placing the PLL in holdover when the quality level of the reference clock is less than the quality level of the state of the PLL, Zhang et al discloses placing the PLL in holdover when the reference clock is unstable (Col. 19, lines 4-6) by monitoring the phase error variation rate of the PLL and determining if the phase variation rates meet the threshold. (Col. 14, lines 11-30) Although Zhang et al does not disclose a varying status message and placing the PLL in holdover based on the varying status message, Zampetti et

al discloses a memory or a control unit monitors the status message (Fig. 1, labels 105,109,107, Col. 5, lines 44-59) and to selectively place the phase locked loop in a holdover condition in response to the status messages (Col. 9, lines 32-39). It would be obvious to one skilled in the art to incorporate a variable status message calculated based on the reference signal as disclosed by Zampetti et al into Zhang et al's invention to prevent phase buildout or transmission errors related to slew rate and amplitude of an individual phase transient event. (Col. 2, lines 41-43 and Col. 9, lines 32-39)

a. **Claim 2**, Zhang et al discloses wherein the instructions stored on the memory (Col. 13, lines 48-51) are capable of causing the processor to selectively place the phase locked loop in the holdover condition (Col. 19, lines 9-26) in response to the status message (Col. 13, lines 64-67 and Col. 14, lines 1-48) regardless of a validity of the reference clock signal. (Col. 19, lines 4-31)
b. **Claim 4** inherits all the limitations of claims 1 and 2.
c. **Claim 5** inherits all the limitations of claim 1.
d. **Claim 7**, Zampetti et al discloses the stratum level can transition among different stratum clocks because of phase buildout. (Col. 5, lines 35-43)
e. **Claim 8** inherits all the limitations of claim 1.
f. **Claim 9** inherits all the limitations of claims 1 and 2.

5. **Claims 10,12-13,15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al (US Patent No.: 6304582) in view of Zampetti et al (US Patent No.: 6943609) and further in view of Dubberley et al (US Patent No.: 5581555).

   a. **Claim 10** inherits all the limitations of claim 1, but claim 1 does not recite a receiver, a framer and a prescaler. Zhang et al discloses a prescaler. (Fig. 3, label scaler prior to phase comparator). Although Zhang et al fails to discloses a framer, Dubberly et al discloses a cascaded parallel phase locked loop comprising a receiver (Fig. 8, label 100), a framer (Fig. 8, label 102) and a prescaler coupled between the framer and PLL. (Fig. 8, label 102 and Fig. 14, labels 525 and 528) It would be obvious to one skilled in the art to incorporate a framer to Zhang et al's invention to provide alternat use of each channel as a data transmission channel, which would allow for support of direct digital services. (Col. 19, lines 18-22)

   b. **Claim 12** inherits all the limitations of claims 1 and 10.

   c. **Claim 13** inherits all the limitations of claim 1.

   d. **Claim 15** inherits all the limitations of claims 1 and 10.

6. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al (US Patent No.: 6304582) in view of Zampetti et al (US Patent No.: 6943609), further in view of Dubberley et al (US Patent No.: 5581555) and further in view of Baydar et al (US Patent No.: 20020097743).

a. **Claim 16** inherits all the limitations of claim 1 and 10 but claims 1 and 10 does not teach a shelf backplane. Baydar et al discloses a shelf backplane and a plurality of shelf elements coupled to the shelf backplane comprising a synchronization of the plurality of shelf elements (Fig. 6, labels 26 and 28, Fig. 7, labels 26 and 28 and Fig. 8), wherein the timing circuit provides a synchronization timing signal to a shelf-plane (Fig. 8, labels 72 and 83 and Fig. 6, labels 26 and 28) and inherently discloses the synchronization timing signal is derived from the first timing signal. (Fig. 8, label 83, page 8, paragraphs [0147][0148][0149], page 9, paragraph [0161] and page 10, paragraph [0164]) It would be obvious to one skilled in the art to incorporate a shelf backplane into Zhang et al's invention to allow transmission and reception from other subscribers with different service formats. (page 2, paragraph [0016])

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 17 and 19** are rejected under 35 U.S.C. 102(e) as being anticipated by Zhang et al (US Patent No.: 6304582).

a. **Claim 17**, Zhang et al discloses generating the timing signal from a reference clock signal in a PLL (Fig. 3, labels 210,240,260,273), monitoring a status

message indicating the quality of the reference clock signal (Col. 14, lines 11-40) and placing the PLL in holdover condition if the quality level indicated by the status message is below a target level (Col. 14, lines 11-30 and Col. 19, liens 4-35), wherein the method is performed in ordered presented as per Fig. 3.

b. **Claim 19**, Zhang et al discloses an expected quality level to place the PLL in holdover. (Col. 14, lines 11-40)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 20-22,24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al (US Patent No.: 6304582) in view of Zampetti et al (US Patent No.: 6943609).

c. **Claim 20** inherits all the limitations of claim 2.

d. **Claim 21** inherits all the limitations of claim 1.

e. **Claim 22** inherits all the limitations of claim 17, but claim 17 does not recite the limitation of selecting the reference clock signal from a primary and secondary reference clock signal. Zhang et al discloses a plurality of T1 clocks and a clock selector. (Fig. 3, labels T1 clocks and clock selector)

f. **Claim 24**, Zhang et al discloses maintaining the PLL in holdover until the reference clock signal is valid and a quality level at or above the target level (Col. 14, lines 11-40 and Col. 19, lines 4-26)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. **Claims 25-26,30-34** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al (US Patent No.: 6304582) in view of Zampetti et al (US Patent No.: 6943609).

a. **Claim 25**, Although Zhang et al does not disclose remaining in holdover for a predetermined period after a reference clock signal having a valid status, Zampetti et al discloses placing the PLL in holdover and remaining in holdover for a period after the reference clock signal is valid. (Col. 9, lines 32-39) It would be obvious to one skilled in the art to incorporate Zampetti et al into Zhang et al's invention to improve transient management in conjunction with high speed digital systems and generate low phase noise high frequency carriers. (Col. 2, lines 41-53)

b. **Claim 26**, Zampetti et al discloses in Col. 8 lines 63-67 and Col. 9, lines 1-3, a multiplexor for selecting the input reference clock signal based on the stratum

level (Fig. 1, labels 105m 107 and 109), which indicates the first reference clock signal will be selected when the stratum level is better than the second reference clock signal. In Col. 8, lines 4-13, Zampetti et al discloses placing the PLL in freerun when the selected signal is good or the stratum level is appropriate. In Col. 9, lines 32-39, the PLL is placed in holdover when an error is detected on the selected input. Although Zampetti et al fails to teach the components of the PLL when free run and in holdover, Zhang et al discloses a phase comparator for outputting the phase error between the reference clock signal and the feedback signal (Fig. 3, labels 210, 275), filtering the first error signal to produce a first control signal (Fig. 3, label 265 and its output), using the first control signal to produce a timing signal (Fig. 3, label 270 and its output), and generating a second feedback in response to the timing signal (Fig. 3, outputs from label 270 and 273). Zhang et al discloses placing the PLL in holdover when the quality of the reference signal is unstable (Col. 19, lines 4-6), generating a holdover control signal (Col. 19, lines 14-21) and generating a timing signal in response to the holdover control signal. (Fig. 3, labels 260 and Dac_in and Col. 19, lines 4-34) Although Zampetti et al fails to teach a target level, it would be obvious to one skilled in the art to select a reference clock signal by comparing the reference signals to a target level instead of selecting the best of the two reference signals based on design choice since the motivation of performing the selection is to use the best possible quality clock

signal based on the options provided so to limit the period in holdover and provide a synchronized timing signal in the least amount of time.

c. **Claim 28** inherits all the limitations of claim 26.

d. **Claim 30** inherits all the limitations of claim 17.

e. **Claim 31** inherits all the limitations of claim 21.

f. **Claim 32** inherits all the limitations of claim 17.

g. **Claim 33** inherits all the limitations of claims 26 and 1.

h. **Claim 34** inherits all the limitations of claim 33.

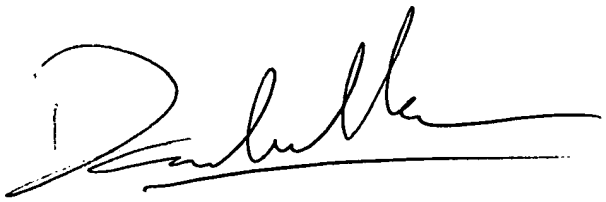
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linda Wong



DAC HA
PRIMARY EXAMINER